addition to the above-described conventional apparatus. As a powerful one of those systems, there is a List Viterbi Algorithm (hereinafter referred to as an LVA). In this system, the Viterbi detector 210 detects the most reliable data sequence (best sequence), the second most reliable data sequence (2nd best sequence), the third most reliable data sequence (3rd best sequence), ... , and the nth most reliable data sequence (nth best sequence), produces these as proposed sequences, or candidates, detects a decoding error of each candidate by use of CRC (Cyclic Redundancy Check) or the like, and generates a decoded output of candidates with no decoding error. The LVA is able to greatly improve the decoding error characteristic of the Viterbi detector. The details of the LVA are described in N. Seshadri et al., "List Viterbi Decoding Algorithms with Applications", IEEE Transactions on Communications, Vol. 42, No. 2/3/4, February/March/April 1994, pp. 313-323. The LVA was originally contrived for application to a communications field such as mobile radio communication, but it has not yet been applied to a magnetic recording/reproducing apparatus. The present invention fundamentally applies the LVA to a magnetic recording/reproducing apparatus as will be described later with respect to various embodiments. However, a simple application of the conventional idea directly to the apparatus cannot achieve high-density recording. This will be described in detail later.--

Delete the paragraph on page 14, line 14, through page 15, line 24, and replace it with the following replacement paragraph:

--Fig. 1 shows the system structure of a digital magnetic recording/reproducing apparatus according to the invention. Referring to Fig. 1, on the recording side, a recording coder 101 converts an input information sequence of 0, 1 of digital data into a high rate code of R=16/17. The recording code, as well known, limits the number of successive 0s to a definite number, thereby preventing the timing extraction and gain control (not shown in Fig. 1) of the reproducing side from being reduced in their performances. The recording coded sequence is then coded for error detection by a CRC coder 102. The CRC can be achieved using a block code produced by adding error detection check bits to the recording coded sequence. Here, the coded sequence is constructed by blocks of much longer CRC block length (more than about 100 bits) so that the substantial coding rate after CRC coding becomes 8/9 or more for high-density recording. If, for example, CRC check bits of 8 bits are added to every 8 units each of which is composed of 17 bits after 16/17 code conversion, the CRC block length is 8 units + 8 bits, or 144 bits, and the coding rate becomes 128/144, or 8/9 as a whole. Thus, the above CRC block structure is able to detect an arbitrary error of, for example, up to 2 bits. Errors can be limited to 2 bits or less by the provision of a precoder 103. The precoder 103